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CactusIC ULP SAR ADC

Functional Description

The CULPADC [Cactus Ultra Low Power ADC] is designed for ultra low power applications where voltage levels must be converted to a 10 bit binary code. Conversion rates up to 50KSPS depending upon external clock frequency. The block is targeted at ultra low power applications such as RFID, biomedical implantable and battery / portable devices. The ADC is useful for housekeeping functions and general voltage monitoring. The ADC can be outfitted with an optional *differential input stage*, or an 8 channel input MUX.

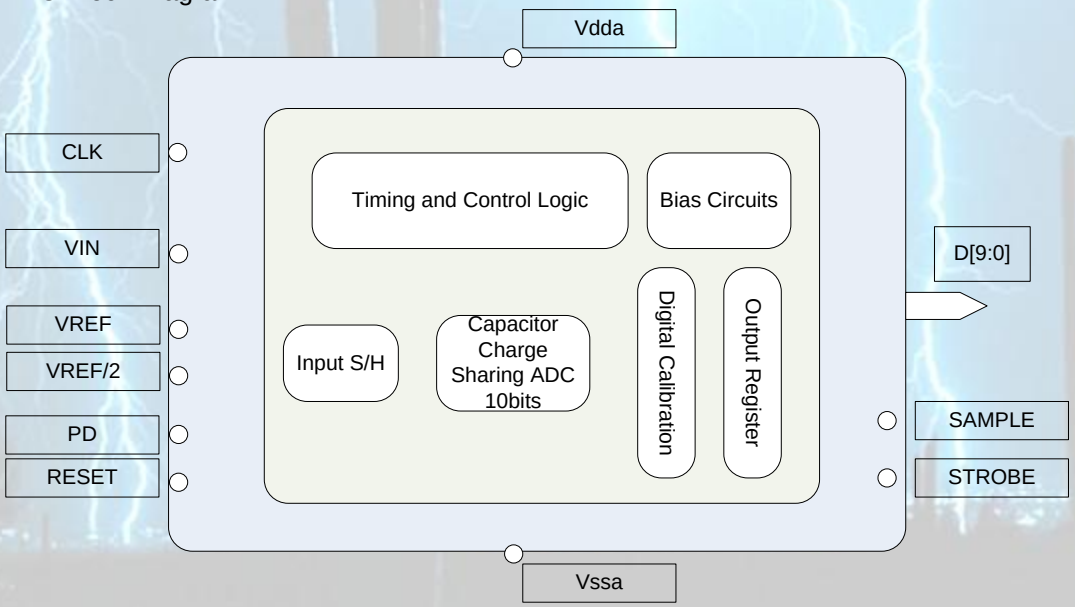
The ADC requires a single power supply from 1.2V to 2.5V and consumes only 5.5uA supply current at 44.1 KSPS with an external 617Khz clock and a 1.2V supply. That is a total power of only 6.6uW. The low power makes it ideal for low power applications where available power is limited.

The CCUPADC can accept an external voltage reference voltage, or it can be used with the CactusIC Sub-Bandgap precision voltage reference, which consumes only 70nW @ Vdd=1V. (See CCUPBGS).

The SAMPLE output is high when the ADC is sampling the input voltage at the VIN port. The STROBE flag goes low when the conversion is completed and the bits can be read.

The ADC is designed in IBM 0.18 processes and is compatible with other general 0.18um CMOS processes and well as other process nodes such as Tower and TSMC.

ADC Block Diagram



Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Positive Supply Voltage	1.2	1.5	1.8	V
V_{SS}	Negative Supply Voltage		0.0		V
T	Temperature	-40	27	125	°C