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CactusIC ULP DSAR ADC**

Functional Description

The DSAR [Digitally Enhanced SAR ADC] is designed for ultra low power applications where voltage levels must be converted to a 10 bit binary code. The DSAR has the unique property that voltage input loading is minimal. The Vin terminal has high input impedance compared to a charge sharing SAR ADC.

Conversion rates are up to 140KSPS depending upon external clock frequency. The block is targeted at ultra low power applications such as RFID, biomedical implantable and battery / portable devices. The ADC is useful for housekeeping functions and general voltage monitoring, and precision temperature sensors. The ADC can be outfitted with an optional *differential input stage*, or an 8 channel input MUX.

The ADC achieves exceptional accuracy with the use of a built-in digital calibration scheme that automatically cancels out any input errors such as device mismatch or offsets.

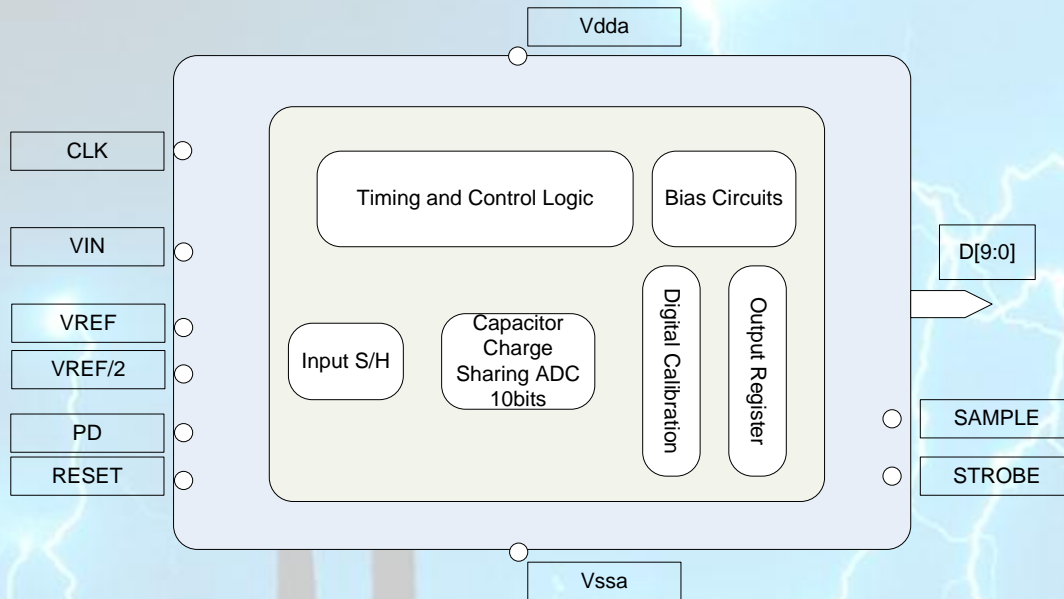
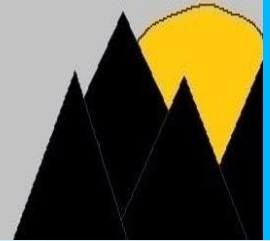
The ADC requires a single power supply from 1.2V to 2.5V and consumes only 2.5uA supply current at 44.1 KSPS with an external 617Khz clock and a 1.2V supply. The low power makes it ideal for low power applications where available power is limited.

The DSAR can accept an external voltage reference voltage, or it can be used with the CactusIC Sub-Bandgap precision voltage reference, which consumes only 70nW @ Vdd=1V.

The SAMPLE output is high when the ADC is sampling the input voltage at the VIN port. The STROBE flag goes low when the conversion is completed and the bits can be read.

The ADC is designed in IBM 0.18 processes and is compatible with other general 0.18um CMOS processes and well as other process nodes such as Tower and TSMC.

ADC Block Diagram



Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Positive Supply Voltage	1.2	1.5	1.8	V
V_{SS}	Negative Supply Voltage		0.0		V
T	Temperature	-40	27	125	°C

